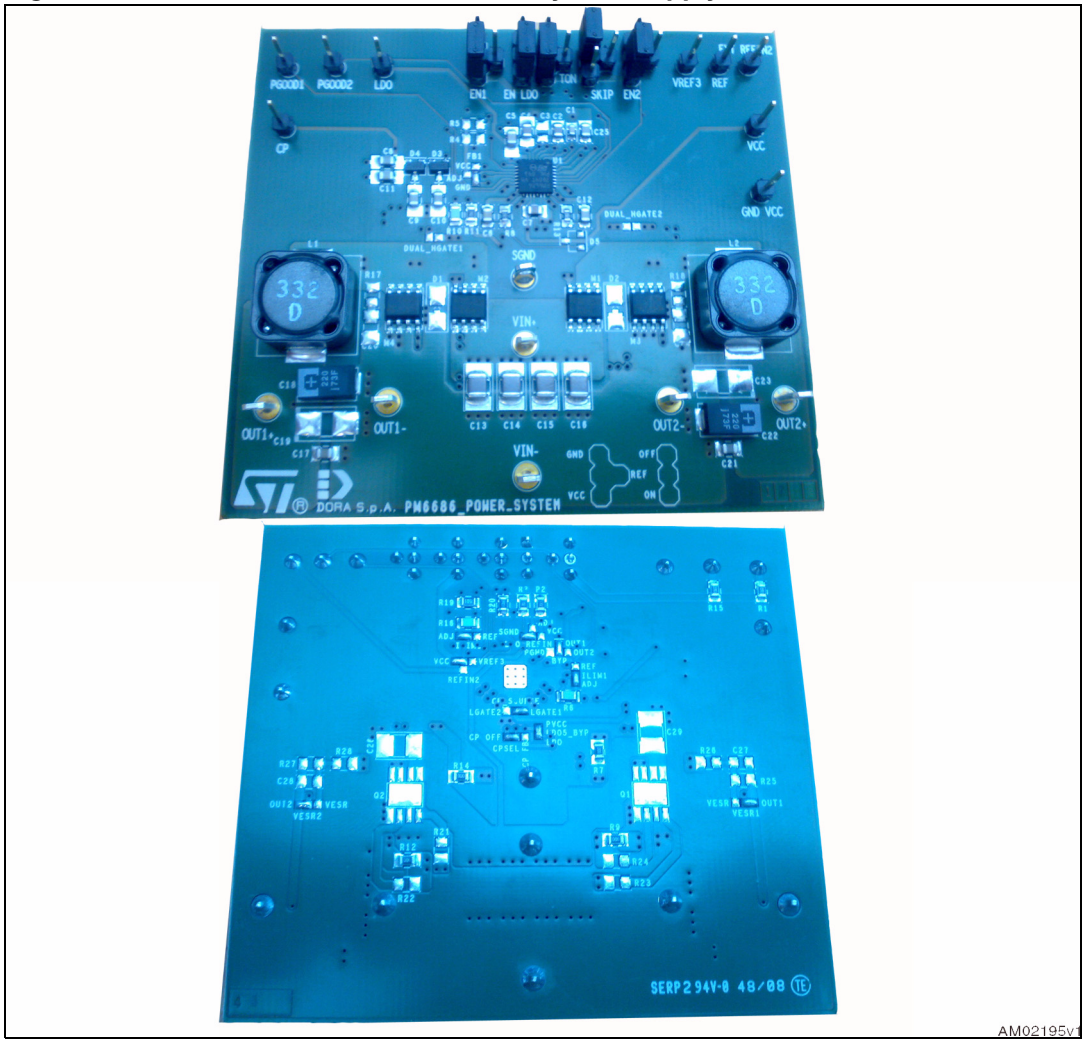
AN2938
Application note

Power system demonstration kit based on the PM6686 dual step-down controller with adjustable voltages and adjustable LDO

Introduction

The PM6686 is a dual step-down controller with adjustable output voltages, adjustable LDO and charge pump circuit for notebook power systems, and this demonstration kit represents a typical application circuit. The demonstration kit for system supply allows the testing of all the PM6686 functions and provides two switching sections, with 5 V (OUT1) and 3.3 V (OUT2) outputs from 8 V to 28 V input battery voltage. The operating switching frequency of the two sections is 400 kHz/300 kHz, respectively. Each switching section delivers more than 8 A of output current. An internal linear regulator can provide 5 V @ 100 mA peak current. The charge pump circuit provides an auxiliary 12 V output voltage.

Figure 1. PM6686 demonstration kit for system supply



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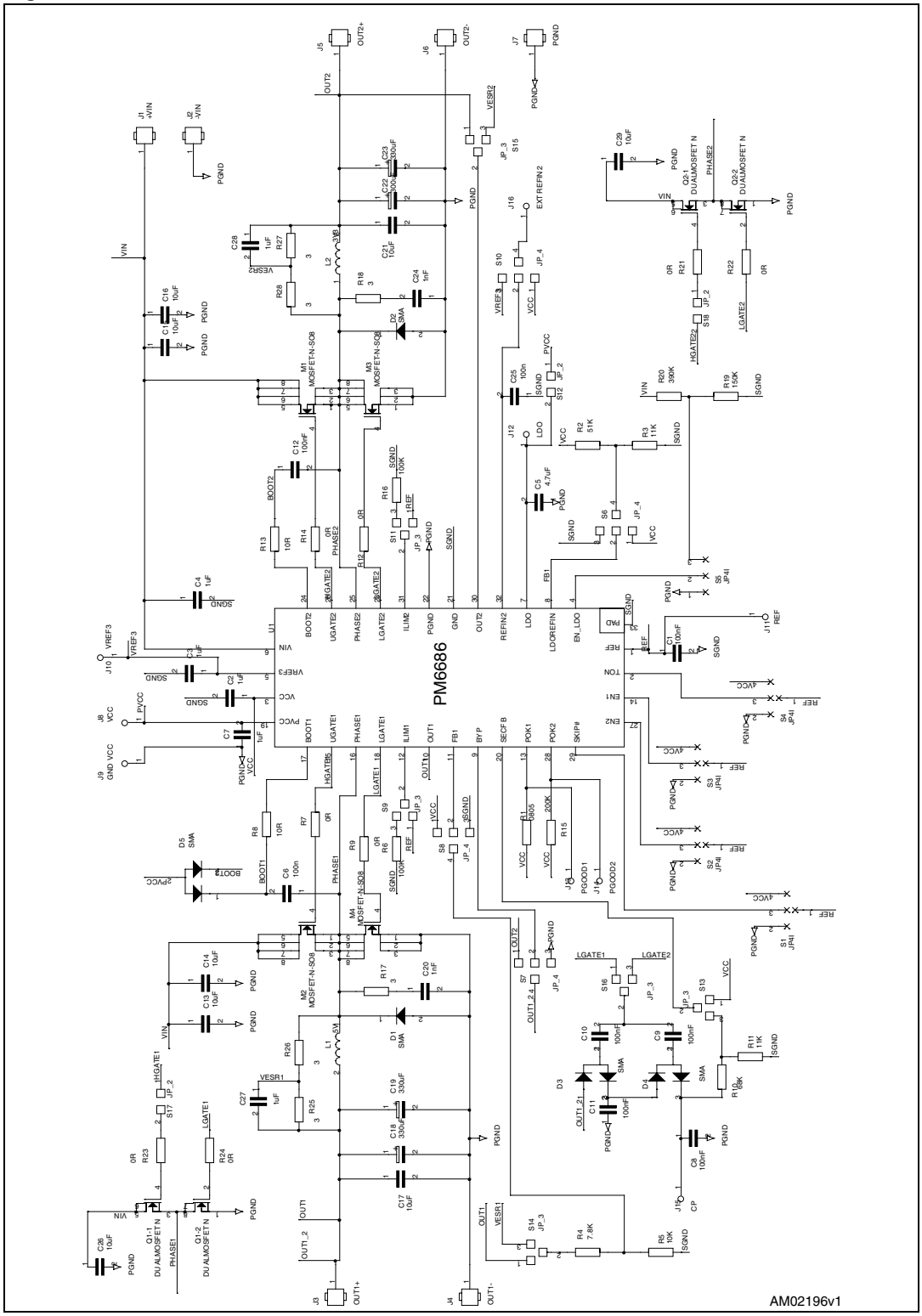
1 Main features

- 5.5 V to 28 V input voltage range
- Dual fixed 1.05 V/3.3 V and 1.5 V/5.0 V outputs or adjustable 0.7 V to 5.5 V (SMPS1) and 0 V to 2.5 V (SMPS2), ±1.5% accuracy over valley regulation
- Low side MOSFETs $R_{DS(on)}$ current sensing and programmable current limit
- Constant on-time control
- Selectable switching frequency
- Soft-start (internally fixed at 2.8 ms) and soft-stop
- Selectable pulse skipping at light loads
- Selectable minimum frequency (33 kHz) in pulse skip mode
- Independent Power Good and EN signals
- Latched OVP and UVP
- Charge pump feedback
- Fixed 3.3 V/5.0 V, or adjustable output 0.7 V to 4.5 V, ±1.5% (LDO): 200 mA
- 3.3 V reference voltage ± 2.0%: 5 mA
- 2.0 V reference voltage ±1.0%: 50 µA

2 Demonstration kit schematic

Figure 2. Demonstration kit schematic



3 Jumper settings

- S7 (BYP jumper) shorted to OUT1
- S8 (FB1 jumper)1 shorted to GND
- S9, S11 (ILIM1,ILIM2 jumper) shorted to resistors
- S12 (LDO to PVCC jumper) shorted
- S10 (REFIN2 jumper) shorted to VCC
- S6 (LDOREFIN jumper) shorted to GND
- S13 (CP_SEL jumper) floating
- S14 (VESR OUT1) open
- S15 (VESR OUT2) shorted to OUT2
- S16 (CP connection) open
- S17-S18 (HS MOS connections) open

4 Component list

Table 1. Component list

Reference	Description	Value
C1	Ceramic capacitor 0603 6.3 V	100 nF
C2	Ceramic capacitor 0603 6.3 V	1 µF
C3	Ceramic capacitor 0603 6.3 V	NM
C4	Ceramic capacitor 0805 25 V	1 µF
C5	Ceramic capacitor 0805 6.3 V	4.7 µF
C6	Ceramic capacitor 0603 6.3 V	100 nF
C7	Ceramic capacitor 0603 6.3 V	1 µF
C8	Ceramic capacitor 0805 16 V	100 nF
C9	Ceramic capacitor 0805 16 V	100 nF
C10	Ceramic capacitor 0805 16 V	100 nF
C11	Ceramic capacitor 0805 16 V	100 nF
C12	Ceramic capacitor 0603 6.3 V	100 nF
C13	Ceramic capacitor 10 µF 1210 35 V	UMKK325BJ106KM Taiyo Yuden
C14	Ceramic capacitor 10 µF 1210 35 V	UMKK325BJ106KM Taiyo Yuden
C15	Ceramic capacitor 10 µF 1210 35 V	UMKK325BJ106KM Taiyo Yuden

Table 1. Component list (continued)

Reference	Description	Value
C16	Ceramic capacitor 10 µF 1210 35 V	UMKK325BJ106KM Taiyo Yuden
C17	Ceramic capacitor 0603 6.3 V	100 nF
C18	POSCAP capacitor 6TPF220ML	
C19	POSCAP capacitor 220 µF 12 mΩ	NM
C20	Ceramic capacitor 0805 50 V 1 nF	NM
C21	Ceramic capacitor 0603 6.3 V	100 nF
C22	POSCAP capacitor 6TPF220ML	
C23	POSCAP capacitor 220 µF 12 mΩ	NM
C24	Ceramic capacitor 0805 50 V 1 nF	NM
C25	Ceramic capacitor 0603 6.3 V 100 nF	100 nF
C26	Ceramic capacitor 10 µF 1210 35 V	NM
C27	Ceramic capacitor 0603 6.3 V 1nF	NM
C28	Ceramic capacitor 0603 6.3 V 1nF	NM
C29	Ceramic capacitor 10 µF 1210 35 V	NM
D1	Schottky diode STPS1L30M	
D2	Schottky diode STPS1L30M	
D3	Schottky diode BAT54SFILM	
D4	Schottky diode BAT54SFILM	
D5	Schottky diode BAT54AFILM	NM
L1	COILCRAFT MSS1260-332	
L2	COILCRAFT MSS1260-332	
M1	Power NMOS SO-8 STS14N3LLH5	
M2	Power NMOS SO-8 STS14N3LLH5	
M3	Power NMOS SO-8 STS15N4LLF3	
M4	Power NMOS SO-8 STS15N4LLF4	
Q1	Power SO-8 dual STS9DNH3LL	Q1
Q2	Power SO-8 dual STS9DNH3LL	Q2
R1	Resistor 0603	220 kΩ
R2	Resistor 0603 0.5%	51 kΩ
R3	Resistor 0603 0.5%	11 kΩ
R4	Resistor 0603 0.5%	NM
R5	Resistor 0603 0.5%	NM
R6	Resistor 0603	200 kΩ
R7	Resistor 0805	0 Ω

Table 1. Component list (continued)

Reference	Description	Value
R8	Resistor 0805	2.2 Ω
R9	Resistor 0805	0 Ω
R10	Resistor 0603	200 kΩ
R11	Resistor 0603	39 kΩ
R12	Resistor 0805	0 Ω
R13	Resistor 0805	2.2 Ω
R14	Resistor 0805	0 Ω
R15	Resistor 0603	220 kΩ
R16	Resistor 0603	200 kΩ
R17	Resistor 0805 3 Ω	NM
R18	Resistor 0805 3 Ω	NM
R19	Resistor 0603	150 kΩ
R20	Resistor 0603	390 kΩ
R21	Resistor 0805	NM
R22	Resistor 0805	NM
R23	Resistor 0805	NM
R24	Resistor 0805	NM
R25	Resistor 0603	NM
R26	Resistor 0603	NM
R27	Resistor 0603	NM
R28	Resistor 0603	NM

5 Demonstration kit layout

Figure 3. PM6686 demonstration board layout - top layer

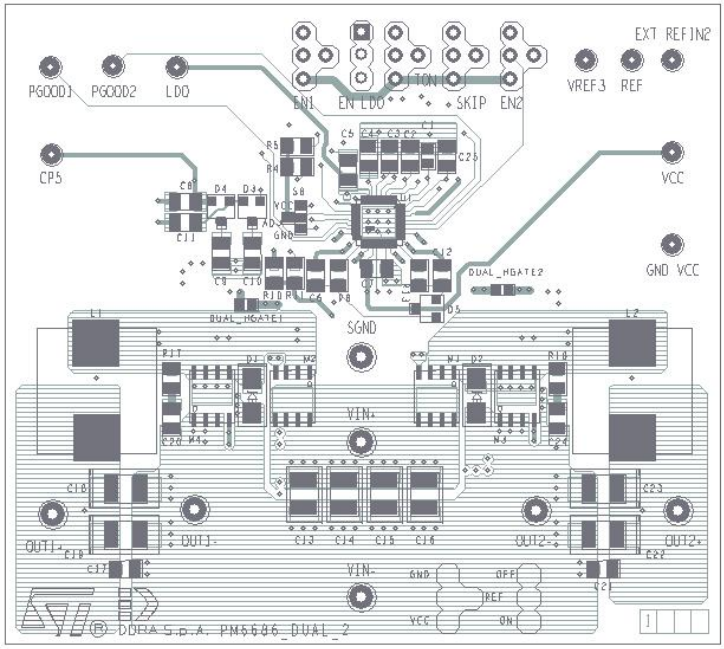


Figure 4. PM6686 demonstration board layout - inner layer 1

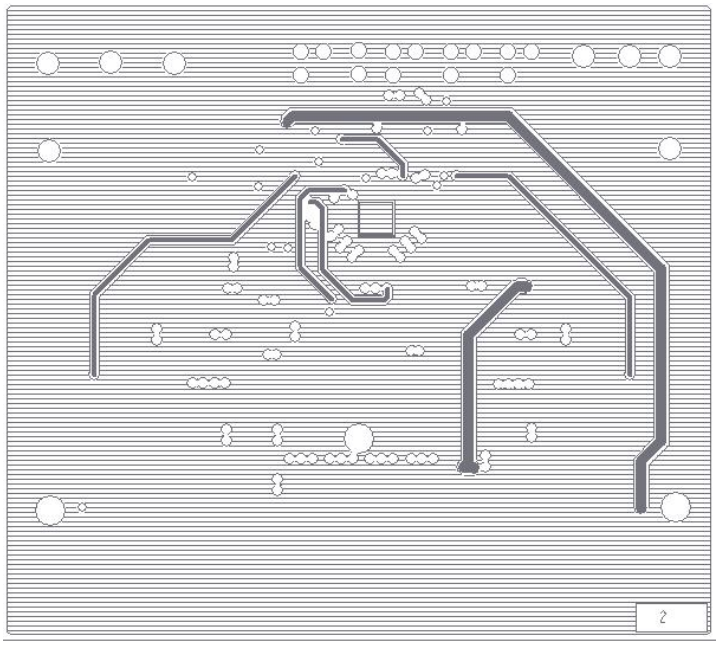


Figure 5. PM6686 demonstration board layout - inner layer 2

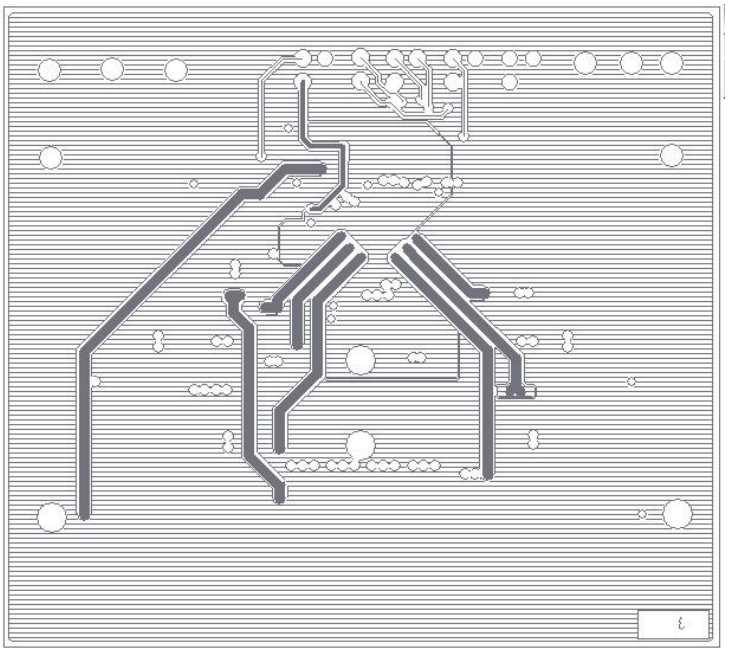
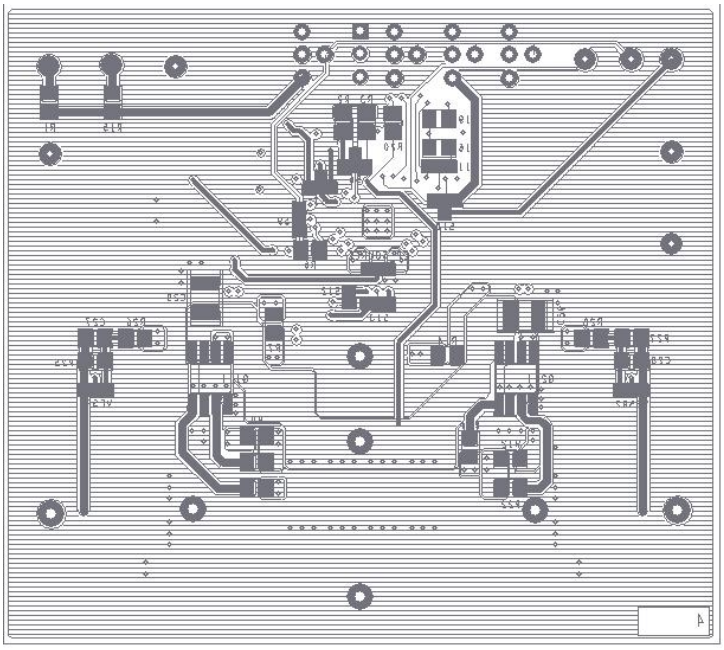


Figure 6. PM6686 demonstration board layout - bottom layer



6 I/O interface

The demonstration board provides the following test points:

Table 2. Demonstration board test points

Test point	Description
VIN+	Input voltage
VIN-	Input voltage ground
LDO	5 V linear regulator output
VCC	Input of the 5 V supply of the device
GND_VCC	Ground of the 5 V supply of the device
OUT1+	OUT1 switching section output
OUT1-	OUT1 switching section output ground
PGOOD1	OUT1 switching section power good
OUT2+	OUT2 switching section output
OUT2+	OUT2 switching section output ground
PGOOD2	OUT2 switching section power good
PGND	Junction pin between PGND and SGND planes
VREF3	3.3 V internal reference output
VREF2	2 V internal reference output
CP	Charge pump output

7 Recommended equipment

- 6 V to 28 V power supply, notebook battery or AC adapter
- Active loads
- Digital multimeters
- 500 MHz four-trace oscilloscope

8 Quick start

1. Connect the VIN+ and VIN- test points of the demonstration board to an external 12 V power supply.
2. Ensure that all jumpers EN1, EN2 and EN_LDO are connected to GND. In this condition all outputs are disabled (shutdown mode).
3. Set jumper EN_LDO at input resistor divider (EN_LDO pin high). The LDO output (LDOREFIN = GND) turns on (standby mode), providing a 5 V voltage.[(a)]
4. Set jumper EN1 at VCC (EN1 pin high). The OUT1 switching controller brings its output into regulation. The PG1 pin goes high after soft-start.
5. Set jumper EN2 at VCC (EN2 pin high). The OUT2 switching controller brings its output into regulation. The PG2 pin goes high after soft-start.
6. In order to load the switching outputs, loads must be connected between the “+” and the “-” output test points, respectively.

a. In this setup, the VCC external supply is directly supplied by output LDO = 5 V. It is possible to disconnect LDO from VCC by disconnecting jumper LDO5V_BYP: in this case VCC external supply is needed before performing the “quick start” procedure.

9 Jumper settings

It is possible to select different working conditions by using the jumpers:

Note: Please note that the jumpers S6, S7, S8, S9, S10, S11, S12 and S13 are already soldered on the demonstration board and there is no need to change them. Refer to the schematic to check their proper connection.

9.1 Switching sections - working modes

Table 3. Jumper S1 SKIP (connect SKIP pin to S1)

Position	Switching sections working mode
GND	If the SKIP pin is tied to ground, a pulse skip mode takes place at light loads. A zero crossing comparator prevents the inductor current from going negative.
VREF2	if the SKIP pin is tied to the VREF pin, a pulse skip mode is enabled with a minimum switching frequency about 25 kHz (ultrasonic mode).
VCC	If the SKIP pin is tied to 5 V, fixed PWM mode occurs. The switching output is in a position to sink and source current from the load.

9.2 Enable switching section 2

Table 4. Jumper S2 EN2 (connect the EN2 pin to S2)

Position	Enable switching section 2
GND	The switching section OUT2 is turned off and all faults are cleared.
VREF2	The switching section OUT2 turns on after the switching section OUT1 reaches regulation.
VCC	The switching section OUT2 is turned on, regardless of the status of the switching section OUT1.

9.3 Enable switching section 1

Table 5. Jumper S3 EN1 (connect EN1 pin to S3)

Position	Enable switching section 1
GND	The switching section OUT1 is turned off and all faults are cleared.
VREF2.	The switching section OUT1 turns on after the switching section OUT2 reaches regulation.
VCC	The switching section OUT1 is turned on, regardless of the status of the switching section OUT2.

9.4 Switching sections - frequency selection (TON)

Table 6. Jumper S4 TON (connect TON pin to S4)

Position	SMPS OUT1	SMPS OUT2
GND	400 kHz	500 kHz
VREF2	400 kHz	300 kHz
VCC	200 kHz	300 kHz

9.5 Linear regulator LDO enable (EN_LDO)

Table 7. Jumper S5 EN_LDO (connect EN_LDO pin to S5)

Position	Linear regulator LDO enable
GND	The LDO is disabled.
VIN though resistor divider	The LDO is enabled. EN_LDO is connected to VIN with a resistor divider. As soon as the input voltage overlaps 5.76 V typ. The LDO regulates the LDO output voltage.

9.6 LDO regulation (LDOREFIN)

Table 8. Jumper S6 LDOREFIN (connect LDOREFIN pin to S6)

Position	LDO regulation
GND	The LDO regulates 5 V.
VREF2	The LDO regulates a voltage equal to two times the voltage at LDOREFIN input.
VCC	The LDO regulates 3.3 V.

9.7 External bypass connections for the linear regulator (BYP)

Table 9. Jumper S7 BYP (connect LDO_SW pin to S7)

Position	External bypass connections for the linear regulator
GND	The internal linear regulator LDO is always on. It can provide an output peak current of 100 mA.
OUT1.	If LDO regulates 5 V and BYP goes higher than 4.74 V, an internal P-channel MOSFET switch connects the BYP pin to the LDO pin, shutting down the LDO internal linear regulator. It can provide an output peak current of 200 mA.
OUT2	If LDO regulates 3.3 V and BYP goes higher than 3.17 V, an internal P-channel MOSFET switch connects the BYP pin to the LDO pin, shutting down the LDO internal linear regulator. It can provide an output peak current of 100 mA.

9.8 OUT1 switching section regulation (FB1)

Table 10. Jumper S8 FB1 (connect FB1 pin to S8)

Position	OUT1 regulation
GND.	OUT1 regulates 5 V.
Ext divider.	OUT1 regulates an adjustable voltage from 0.7 V to 5.5 V, programmable with the external divider R4, R5.
VCC	OUT1 regulates 1.5 V.

9.9 Current limit of OUT1 switching section (ILIM1)

Table 11. Jumper S9 ILIM1 (connect ILIM1 pin to S9)

Position	OUT1 regulation
External resistor	The threshold voltage of ILIM1 is compared with 1/10th of the GND-PHASE1 drop during the off time to determine a valley current limit.
VREF2.	The internal threshold voltage of the current limit comparator is set to 200 mV.

9.10 OUT2 switching section regulation (REFIN2)

Table 12. Jumper S10 REFIN2 (Connect REFIN2 pin to S10)

Position	OUT2 regulation
GND	OUT2 regulates 1.05 V.
Reference EXT REFIN2	OUT2 regulates the reference voltage at EXT_REFIN2 pin.
VCC.	OUT2 regulates 3.3 V.

9.11 Current limit of OUT2 switching section (ILIM2)

Table 13. Jumper S11 ILIM2 (connect ILIM2 pin to S11)

Position	OUT2 regulation
External resistor	The threshold voltage of ILIM2 is compared with 1/10th of the GND-PHASE2 drop during the off time to determine a valley current limit.
VREF2	The internal threshold voltage of the current limit comparator is set to 200 mV.

9.12 Connection of LDO output (=5 V) to the PVCC pin (LDO5V_BYP)

Table 14. Jumper S12 LDO5V BYP (connect PVCC pin to S12)

Position	Connection of LDO output (= 5 V) to PVCC pin
SHORTED	If LDOREFIN=GND, LDO regulates 5 V. In this case PVCC and VCC pin of the device can be supplied with the LDO by setting this jumper in this position.
OPEN	PVCC and VCC need to be supplied with an external 5 V source. The LDO is disconnected from PVCC pin.

9.13 Regulation of the charge pump CP (CP SEL)

Table 15. Jumper S13 CP SEL (connect CP_FB pin to S13)

Position	Regulation of the charge pump CP
VCC Or left floating	The charge pump controller is disabled.
External divider	The charge pump regulates the voltage set with the external divider.

9.14 Output 1, virtual ESR connection

Table 16. Jumper S14 VESR1

Position	Virtual ESR enable circuit for section 1
Left floating	Virtual ESR circuit is disabled.
VESR1	Virtual ESR circuit is enabled.

9.15 Output 2, virtual ESR connection

Table 17. Jumper S15 VESR2

Position	Virtual ESR enable circuit for section 2
OUT2	Virtual ESR circuit is disabled.
VESR2	Virtual ESR circuit is enabled.

9.16 LGATE source for charge pump circuit

Table 18. Jumper S16 CP_SOURCE

Position	Source of the charge pump CP
LGATE1	The charge pump circuit is supplied by low side driver of section 1.
LGATE2	The charge pump circuit is supplied by low side driver of section 2.

9.17 MOSFET dual option, high side connection section 1

Table 19. Jumper S17 DUAL_GATE_1

Position	Connection of high side MOS (dual configuration)
SHORTED	Short this jumper to connect the HGATE1 drive to the MOSFET gate if dual MOSFETs are mounted.
OPEN	Leave this jumper open if MOSFET in single package is used.

9.18 MOSFET dual option, high side connection section 2

Table 20. Jumper S18 DUAL_GATE_2

Position	Connection of high side MOS (dual configuration)
SHORTED	Short this jumper to connect the HGATE2 drive to the MOSFET gate if dual MOSFET are mounted.
OPEN	Leave this jumper open if MOSFET in single package is used.

10 Test setup and performance summary

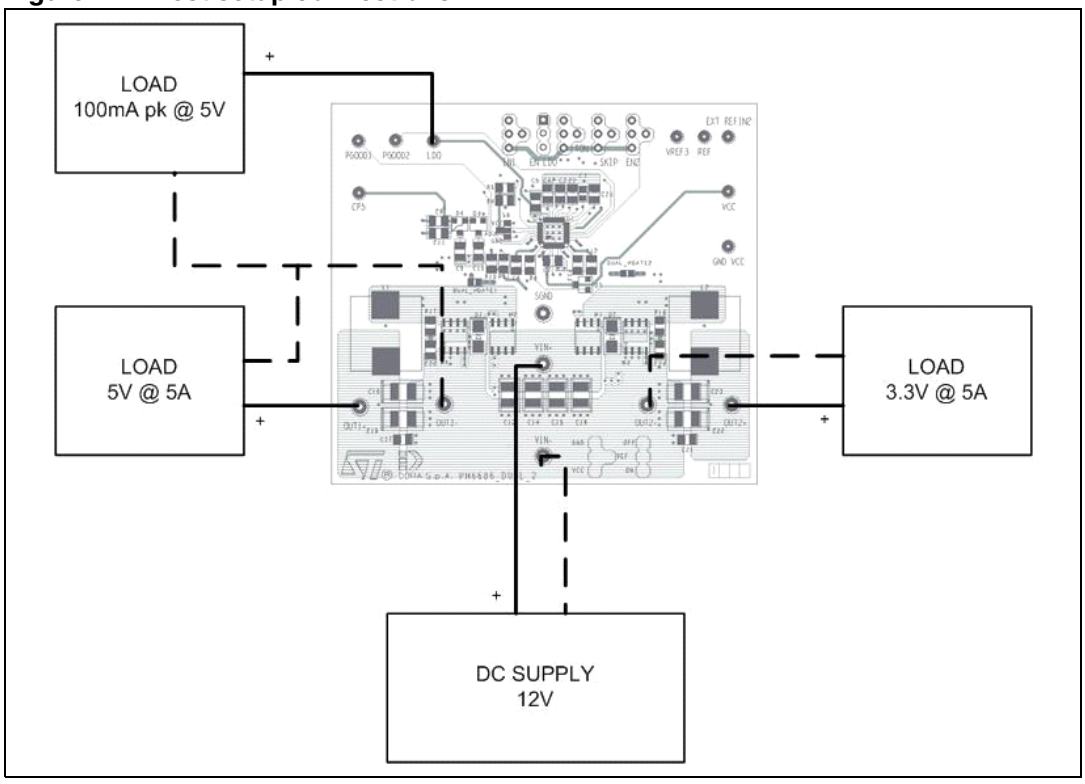
10.1 Test setup

The PM6686 demonstration board has the following input/output connections:

- 12 V input through VIN+ and VIN- connectors
- OUT1 output through OUT1+ and OUT1- connectors
- OUT2 output through OUT2+ and OUT2- connectors
- LDO linear regulator output through LDO connector
- charge pump output CP through CP connector

A power supply capable of supplying at least 6 A should be connected to VIN+, VIN- and two active loads should be connected respectively to OUT1+, OUT1- and OUT2+, OUT2-.

Figure 7. Test setup connections



11 Representative waveforms

11.1 Operating modes-skip, NA skip, PWM

The following illustrations show the relevant waveforms of a switching section and is provided to underline the behavior of the device in pulse skip mode, no-audible skip mode and forced PWM mode working conditions

Figure 8. SMPS pulse skip mode, no load

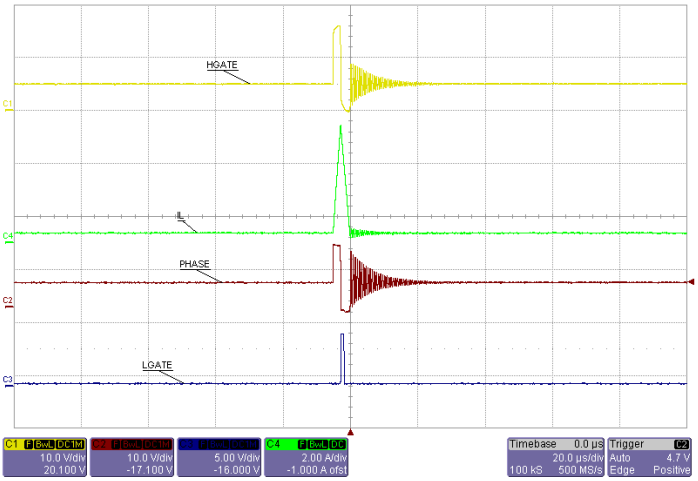


Figure 9. SMPS no-audible skip mode, no load

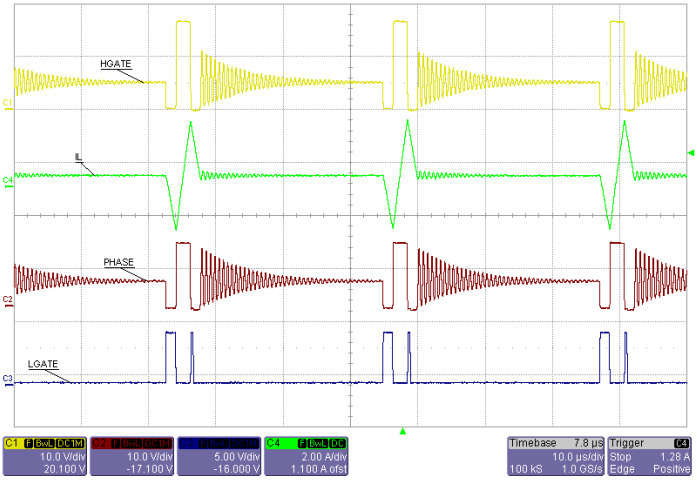
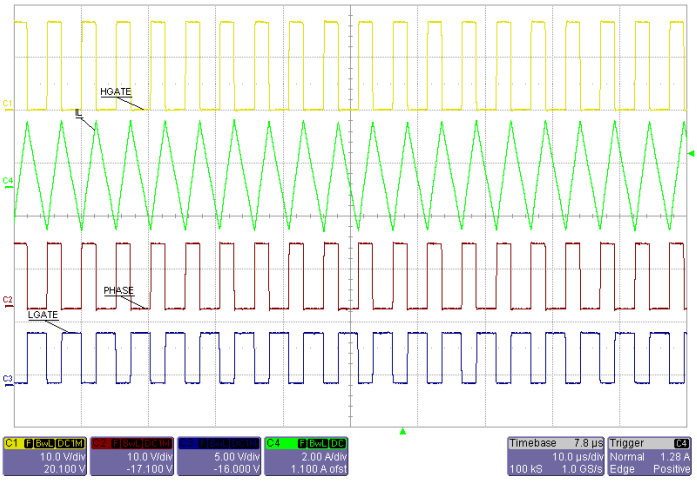


Figure 10. SMPS PWM mode, no load



11.1.1 Switching sections soft-start and soft-end

Figure 11 and *Figure 12*, *Figure 13* and *Figure 14* show the soft-start and soft-end waveforms, respectively.

The PM6686 has an independent internal digital soft-start for each switching section. During the soft-start phase, the internal current limit increases from 25% to 100% in increments of 25% to prevent the inductor reaching an excessive value.

Figure 11. Section 1 soft-start waveforms; 8 A constant current load applied

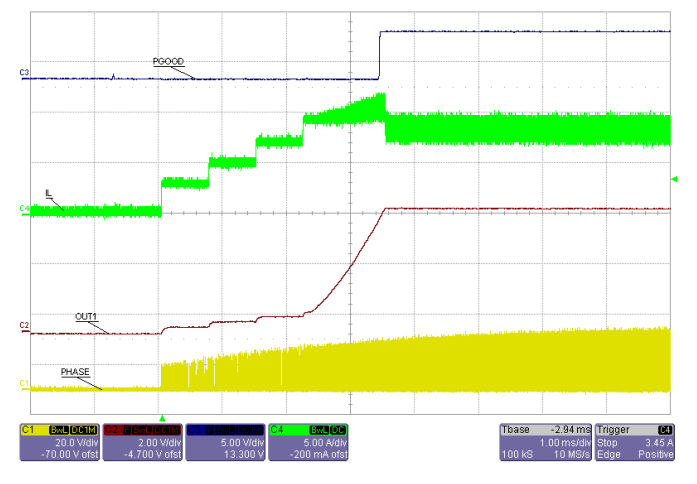
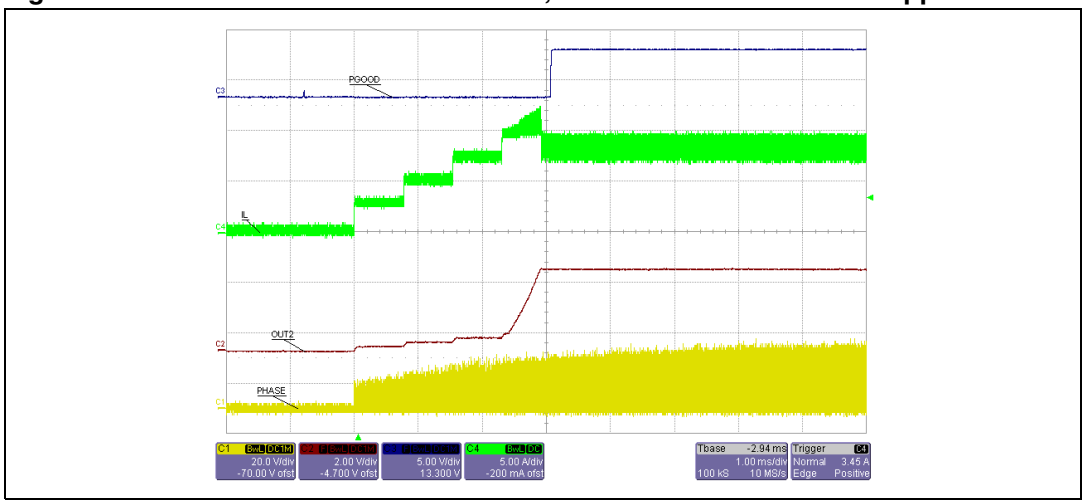


Figure 12. Section 2 soft-start waveforms; 8 A constant current load applied



When the EN pin is driven below the turn-off threshold, the section starts performing a soft-end. The output is connected to ground with an internal 24 Ω (typ.) power MOSFET, so the output is discharged softly. *Figure 13* and *Figure 14* show the soft-end for the two sections.

Figure 13. OUT1 soft-end, no load

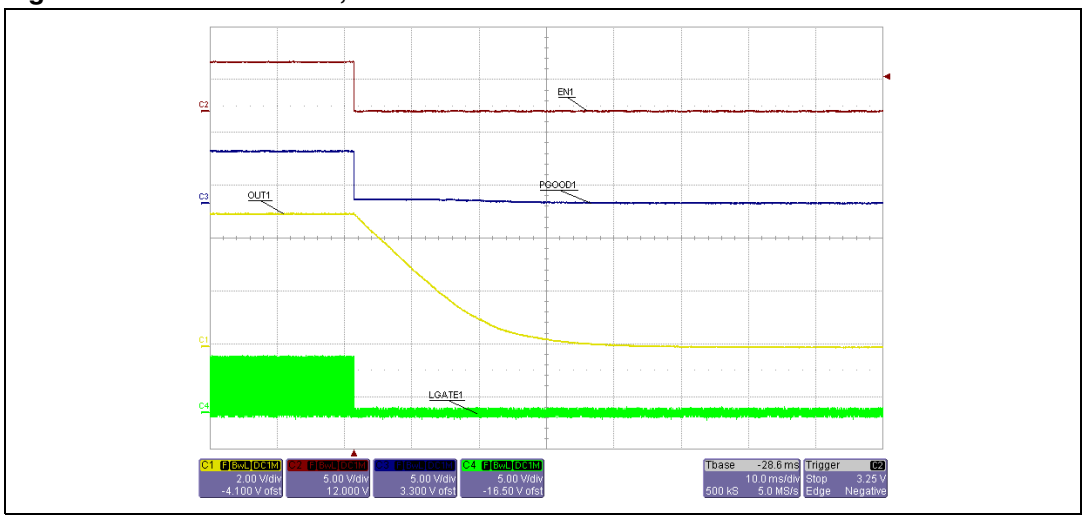
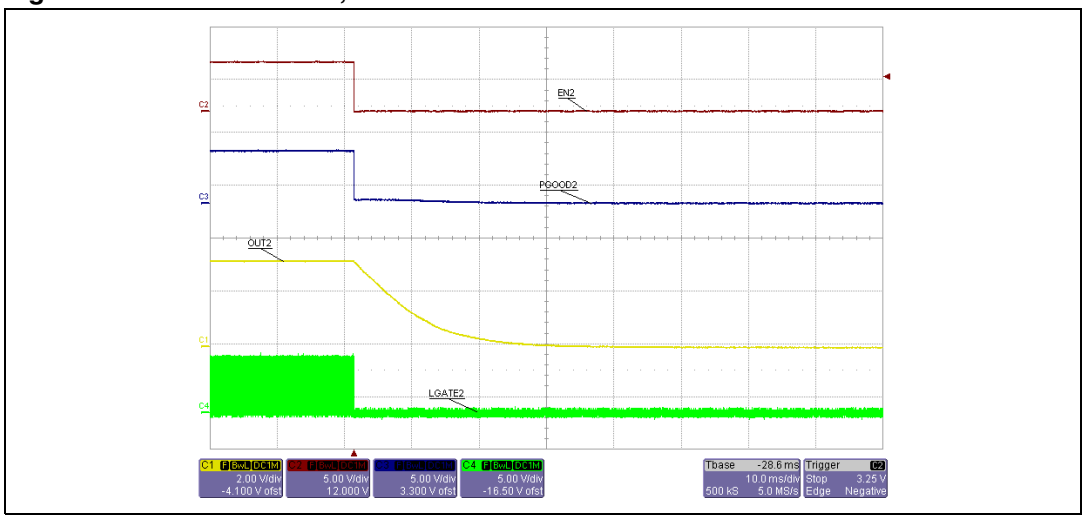


Figure 14. OUT2 soft-end, no load



A power-up sequence for the switching sections can be selected by connecting one EN pin to VREF2.

The section with the EN pin connected to VREF2 begins the soft-start only when the other section is in regulation (its PGOOD is high) and makes a soft-end suddenly when the other section is turned off (*Figure 15* and *Figure 16*).

Figure 15. Tracking soft-start EN2 connected to VREF2, no loads applied

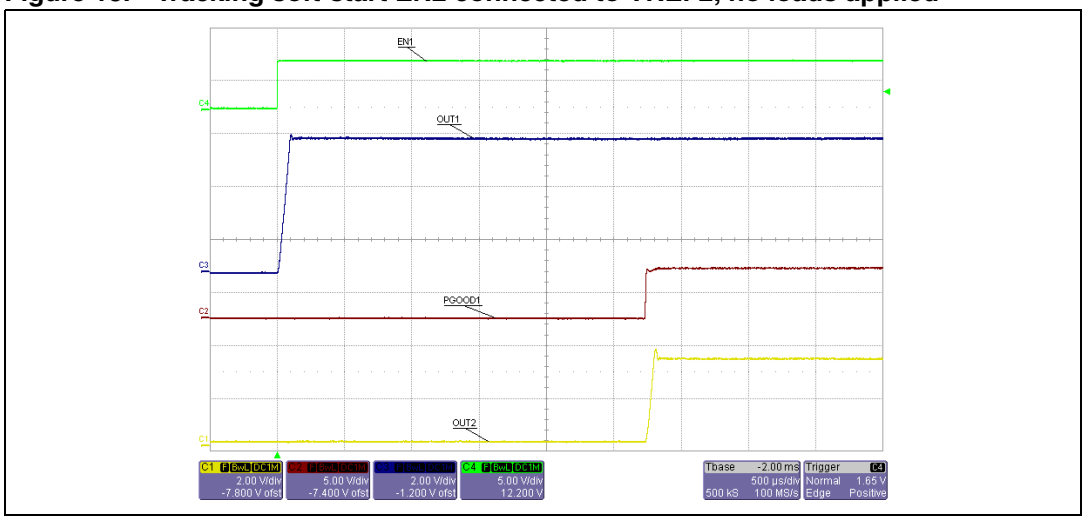
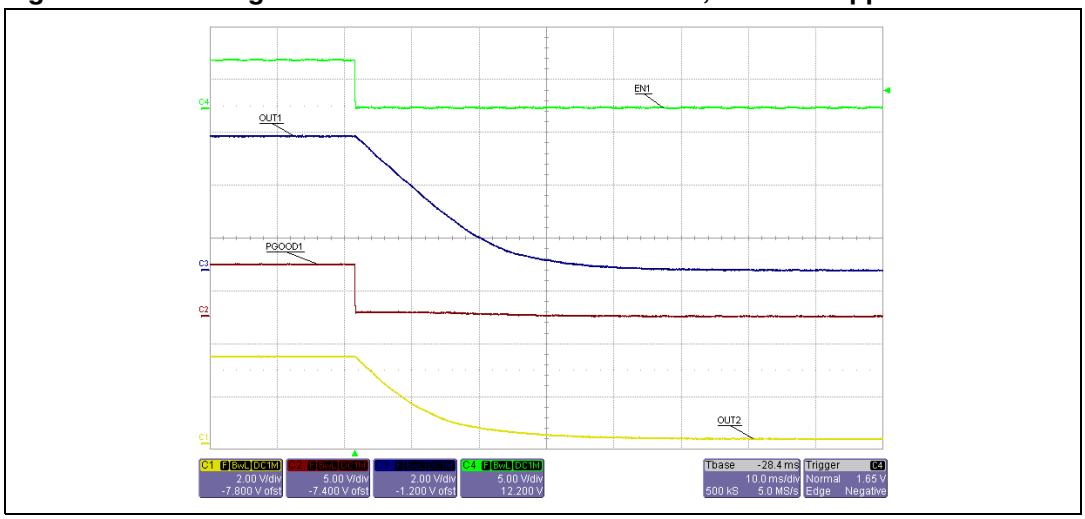


Figure 16. Tracking soft-end EN2 connected to VREF2, no loads applied



11.1.2 Load transient

The illustrations below show the load transient performance both in skip mode and in forced PWM.

Figure 17. OUT1 = 5 V PWM load transient 2 A/µs 0-5 A

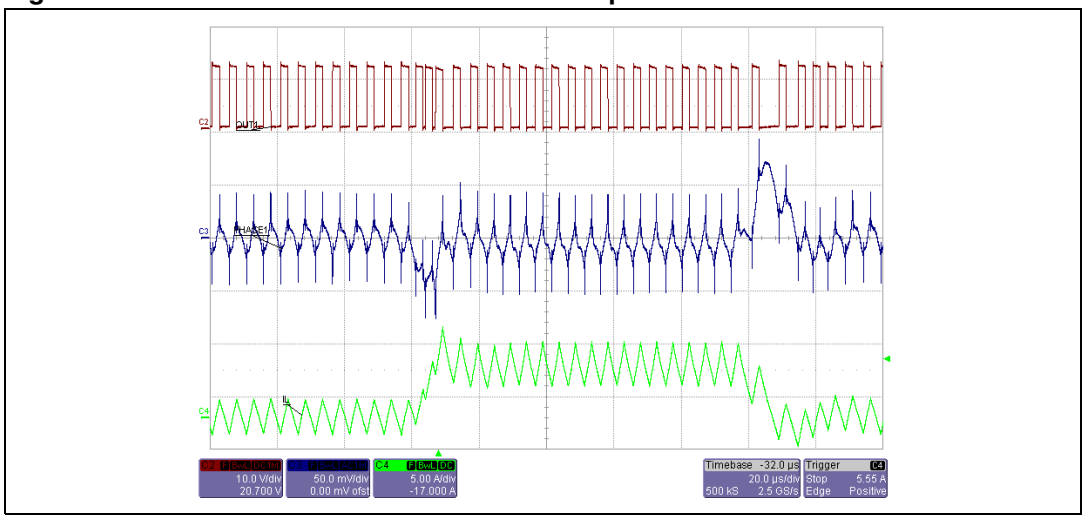


Figure 18. OUT2 = 5 V skip load transient 2 A/µs 0-5 A

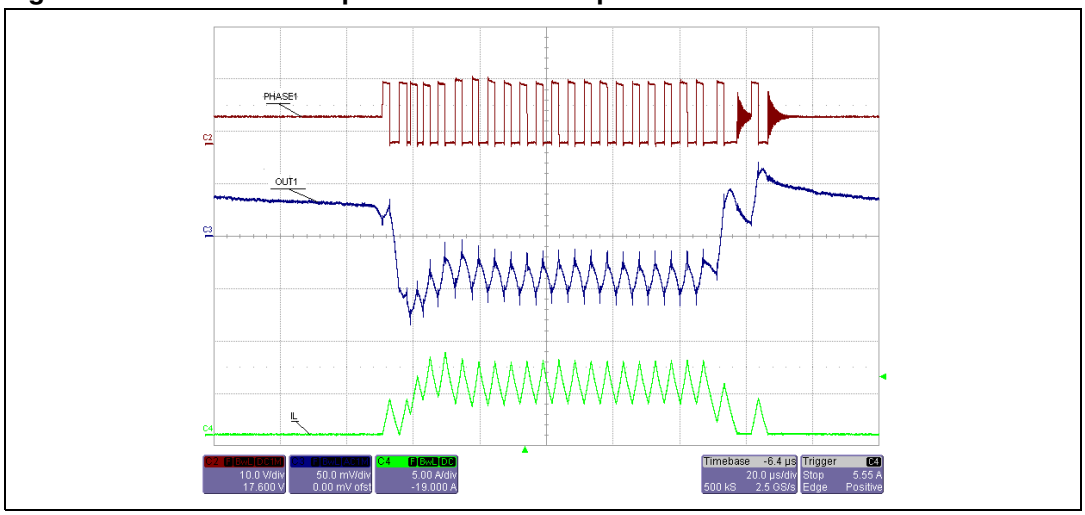


Figure 19. OUT2 = 3.3 V PWM load transient 2 A/µs 0-5 A

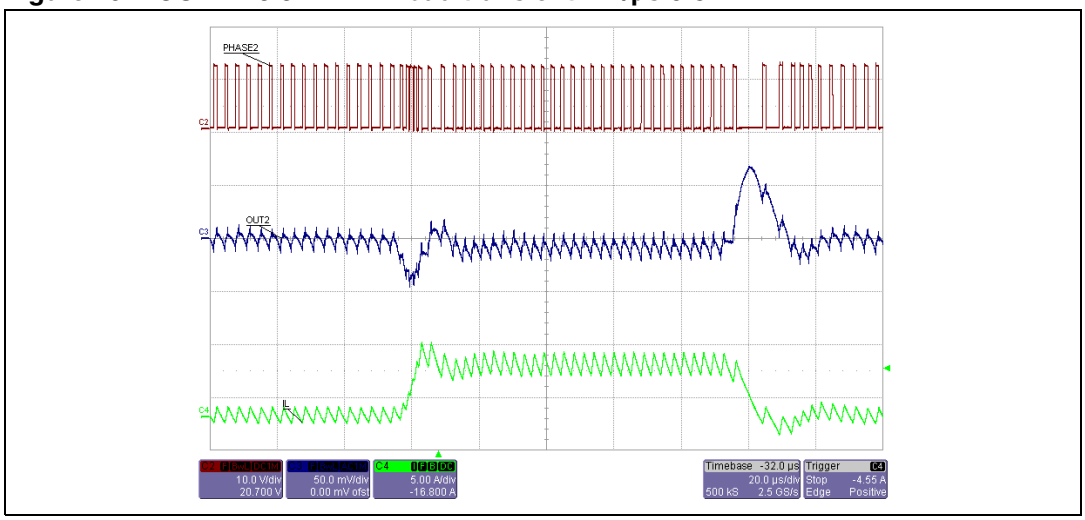
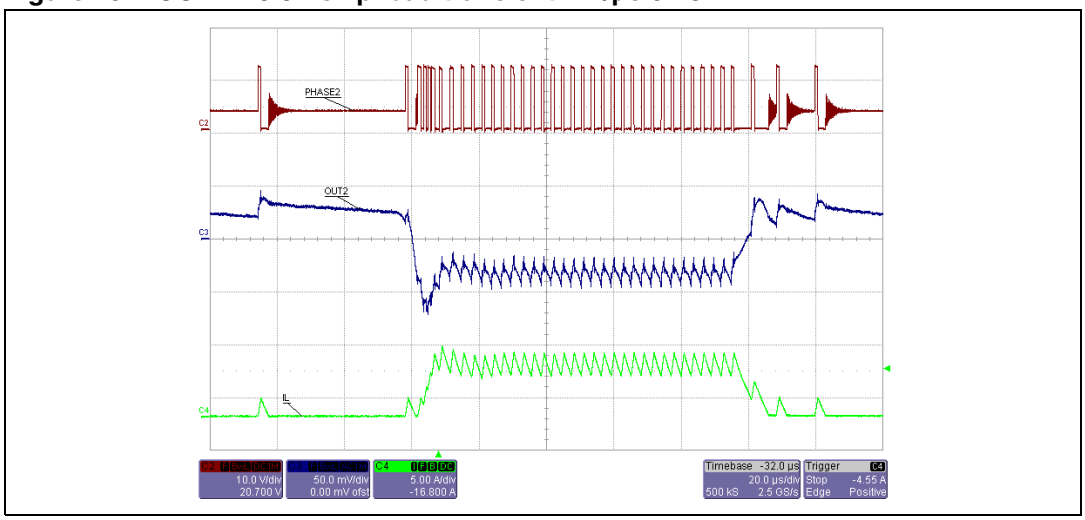


Figure 20. OUT2 = 3.3V skip load transient 2 A/µs 0 - 5 A

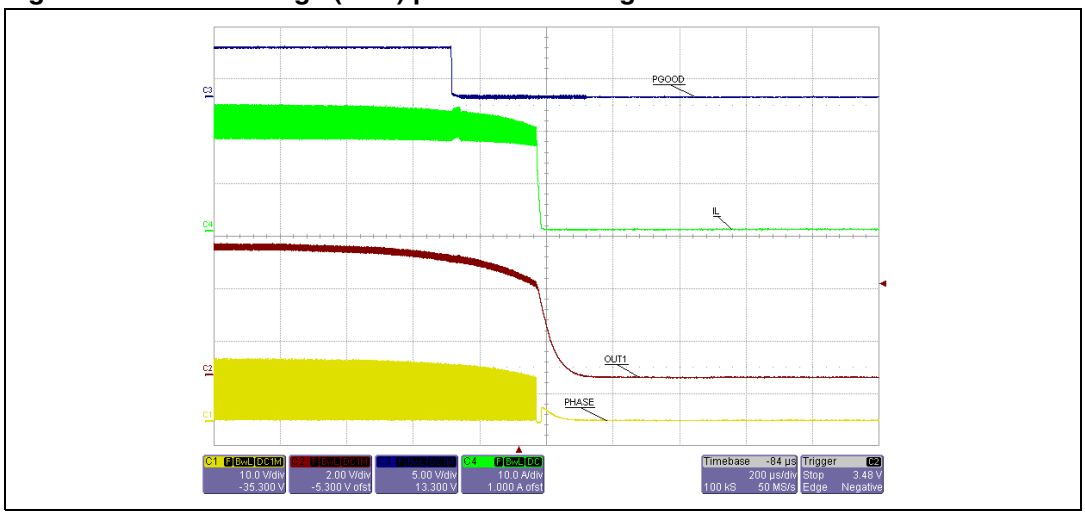


11.1.3 Fault management: overvoltage and undervoltage

The PM6686 provides fault protection for the switching section against undervoltage and overvoltage.

Figure 21 shows the undervoltage fault management. If, during regulation, the output voltage drops below 70% of the nominal value, an undervoltage latched fault is detected. The controller performs a soft-end procedure. The undervoltage fault is reset by toggling the EN pin or by cycling the V_{IN} (this action performs a power on reset [POR]).

Figure 21. Undervoltage (UVP) protection management



The PM6686 provides latched overvoltage protection (OVP). If the output voltage rises above the +111% typ. from the nominal value for section 1 and above the +116% typ. for section 2, latched OVP protection is activated. The controller tries to pull down the output voltage down to 0 V, working in PWM. The current is limited by the negative current limit. The low side MOSFET is kept on when the output voltage is about 0 V. This management prevents high negative undervoltage of the output rail that may damage the load (*Figure 22*).

If the EN signal is pulled low, the low side MOSFET is still high, keeping the output to ground thus preventing any damage to the load if the cause of the overvoltage is still present (*Figure 23*).

The protection is latched and this fault is cleared by toggling the EN pin of the section, or cycling the V_{IN}.

Figure 22. Overvoltage protection management

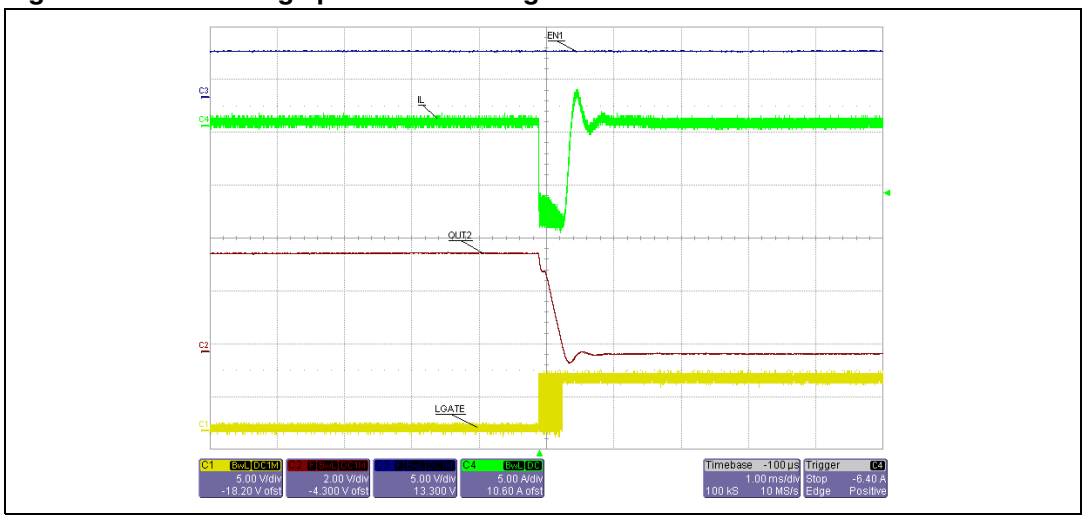
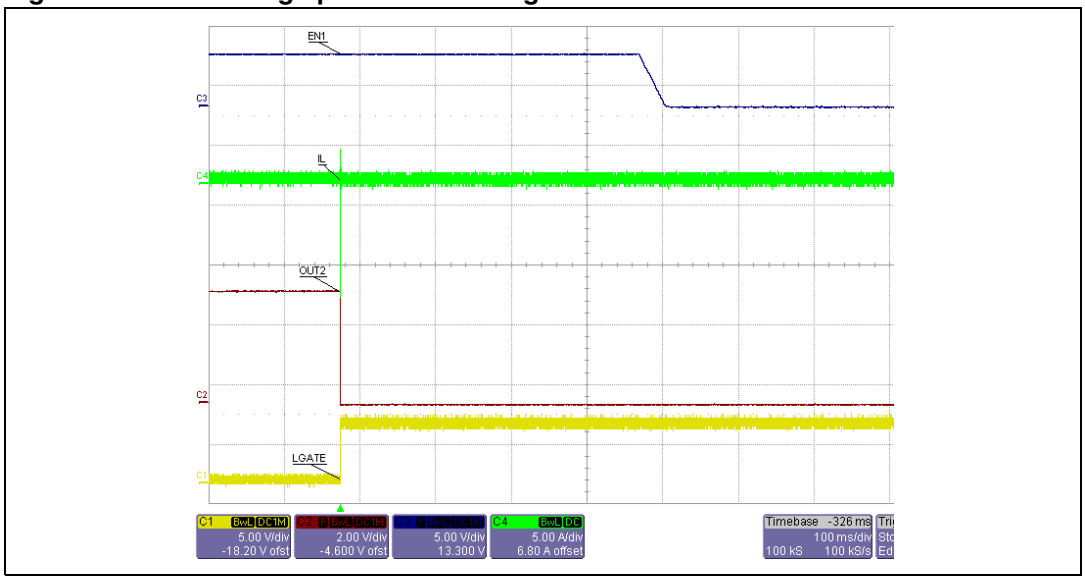


Figure 23. Overvoltage protection management



11.2 Typical operating characteristics

11.2.1 OUT1 and OUT2 output efficiency vs load current

Figure 24 and *Figure 25* show the efficiency versus load current in PWM mode, skip mode and no-audible skip mode for different input voltage values:

- GREEN: 7 V
- BLUE: 12 V
- RED: 18 V

Figure 24. Efficiency OUT1 = 5 V $T_{ON} = V_{CC}$

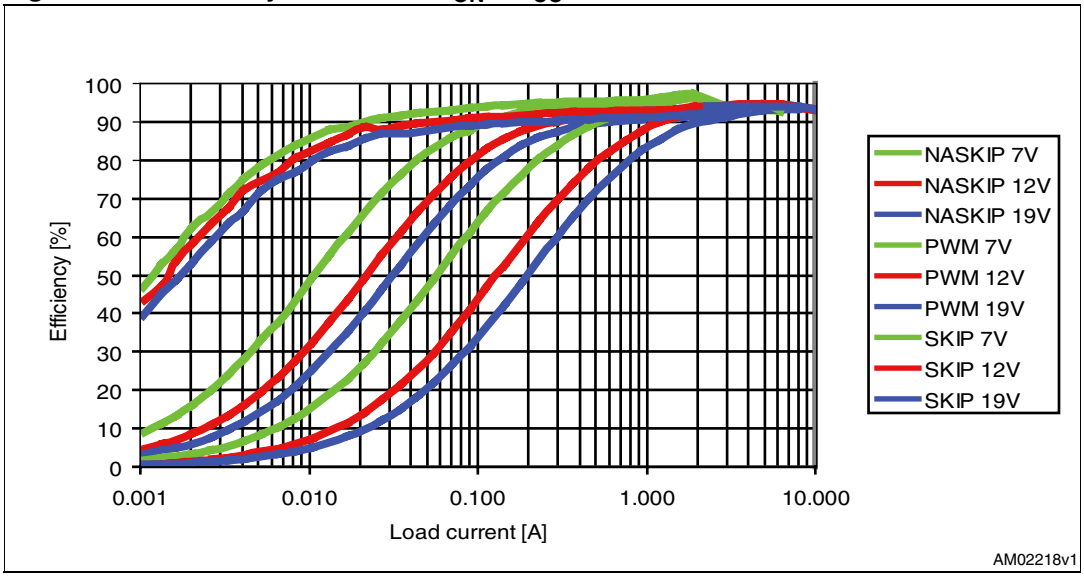
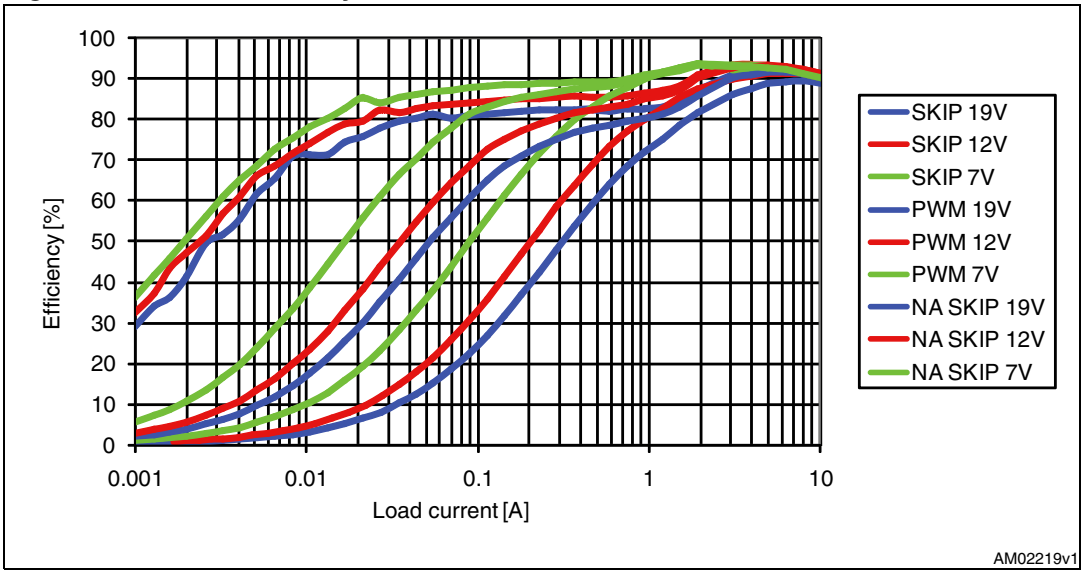


Figure 25. OUT2 efficiency



11.2.2 OUT1 and OUT2 switching frequency vs. load current

Figure 26 and *Figure 27* show the switching frequency versus load current in PWM mode, skip mode, NA skip mode. T_{ON} is connected to V_{CC}.

Figure 26. Switching frequency vs. load _OUT1 = 5 V $T_{ON} = V_{CC}$

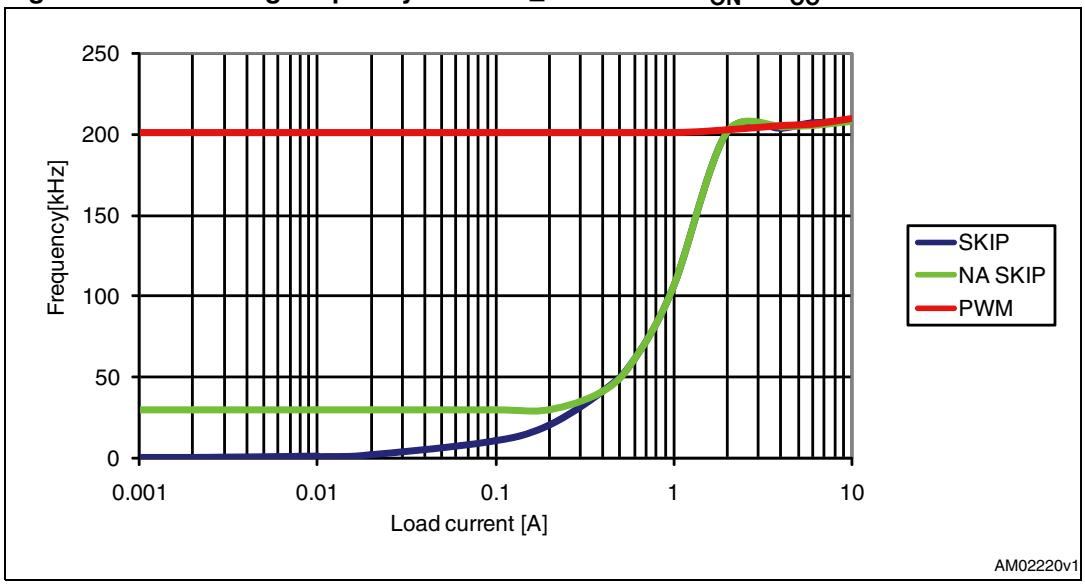
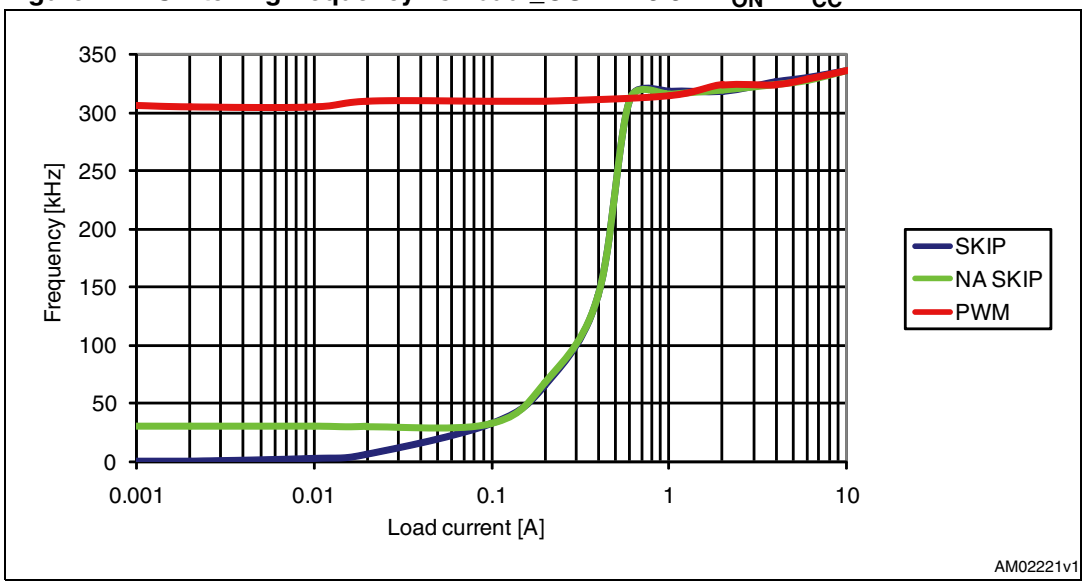


Figure 27. Switching frequency vs. load _OUT2 = 3.3 V $T_{ON} = V_{CC}$



11.2.3 OUT1 and OUT2 output voltage vs. load current

Figure 28 and *Figure 29* show the load regulation of the switching sections' output voltages. The output voltage is measured versus the load current. T_{ON} is connected to V_{CC}.

Figure 28. Load regulation OUT1 = 5 V T_{ON} = V_{CC}

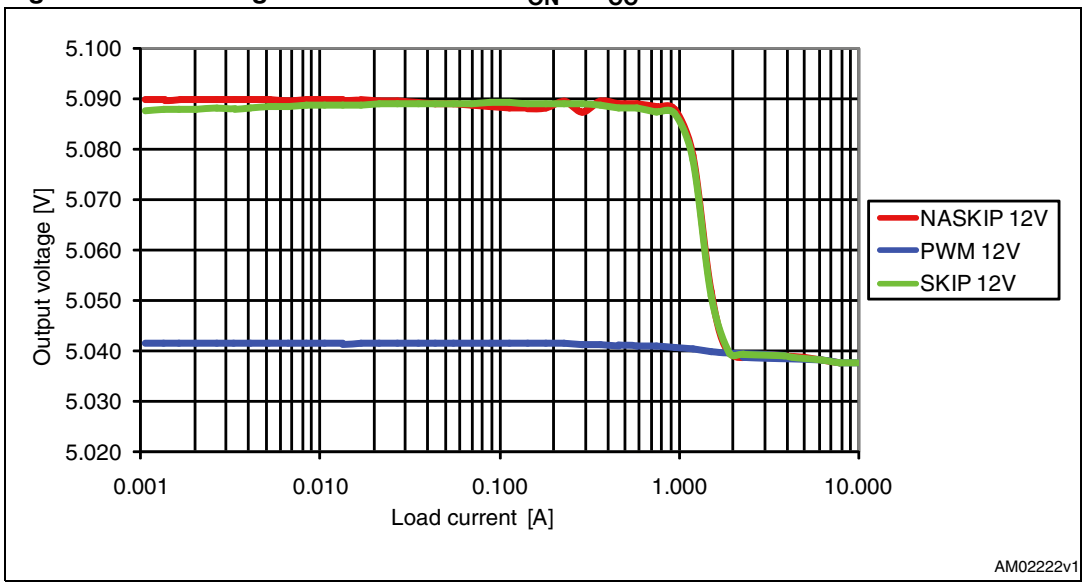
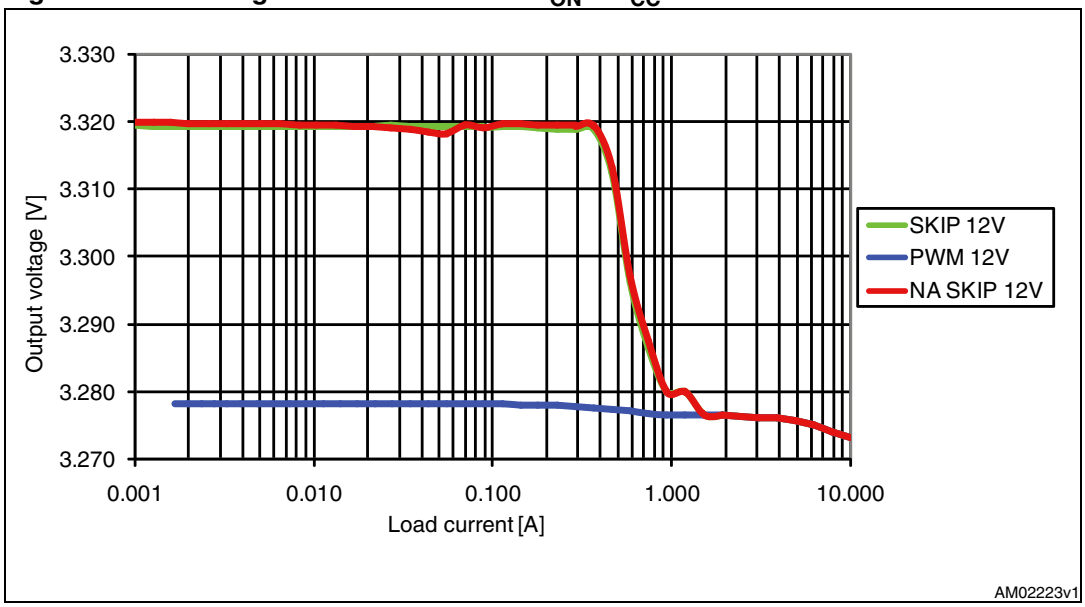


Figure 29. Load regulation OUT2 = 3.3 V T_{ON} = V_{CC}



11.2.4 Power consumption analysis

To measure the device consumption under real working conditions, an external power supply (+5 V) is connected to PVCC. Currents absorptions from VIN and from VCC are measured in the three different operating modes with no load applied at the outputs.

Figure 30. PWM no load input currents vs. input voltage

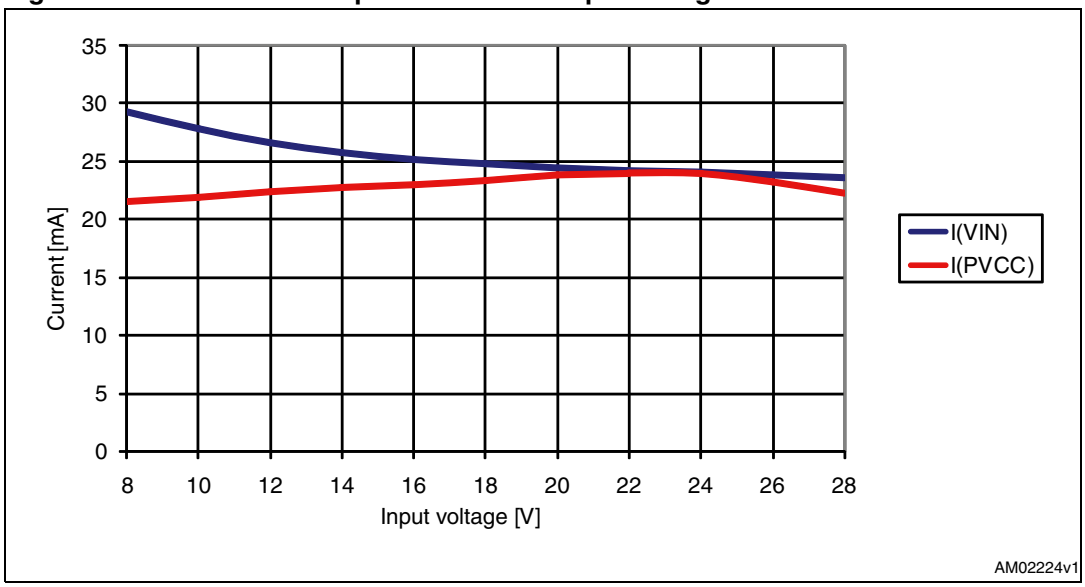


Figure 31. Skip no load input currents vs. voltage

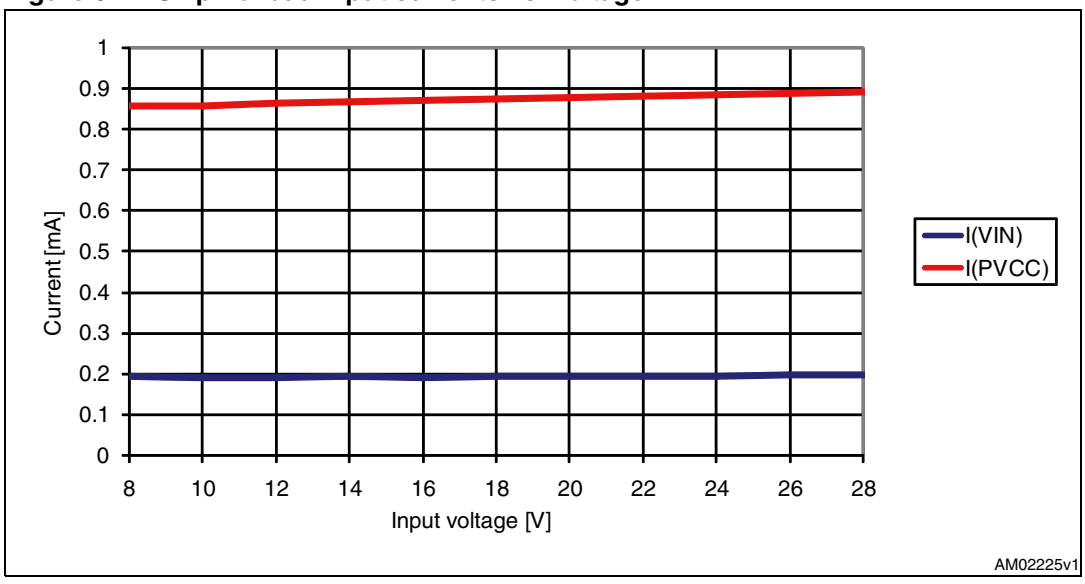
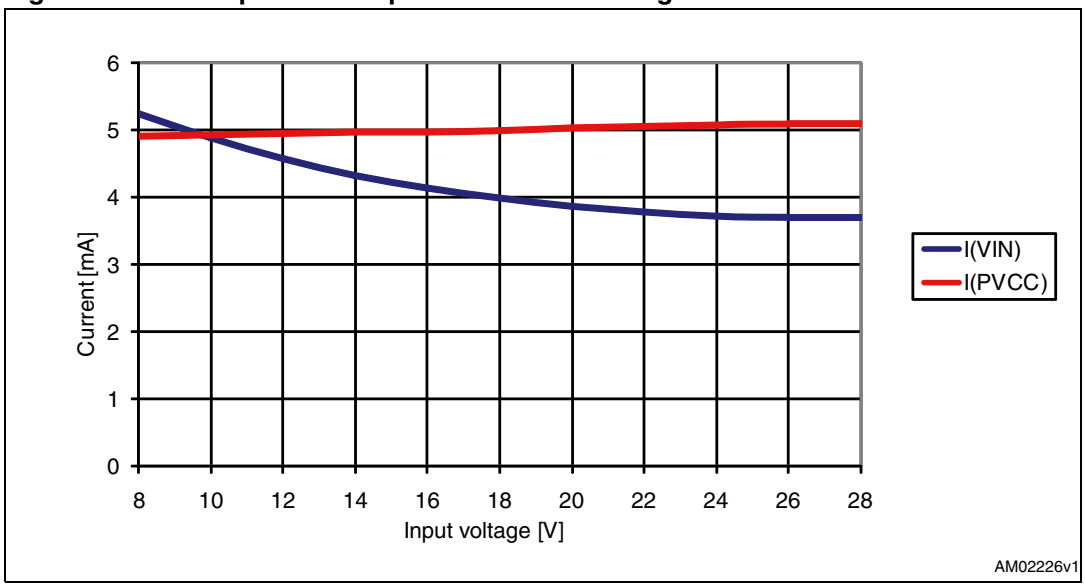


Figure 32. NA skip no load input currents vs. voltage



The following figures represent the current absorption from VIN in standby and shutdown condition. In standby mode, the switching sections are off while the LDO is on (EN1= EN2 = low, EN_LDO = high). In shutdown mode, the switching sections and the LDO are off (EN1 = EN2 = EN_LDO = low).

Figure 33. Input current consumption vs. input voltage

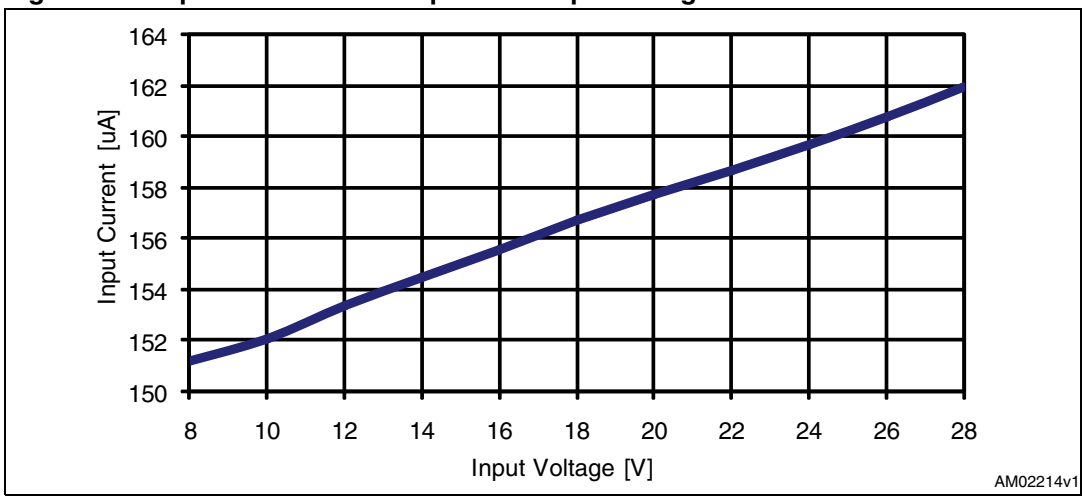
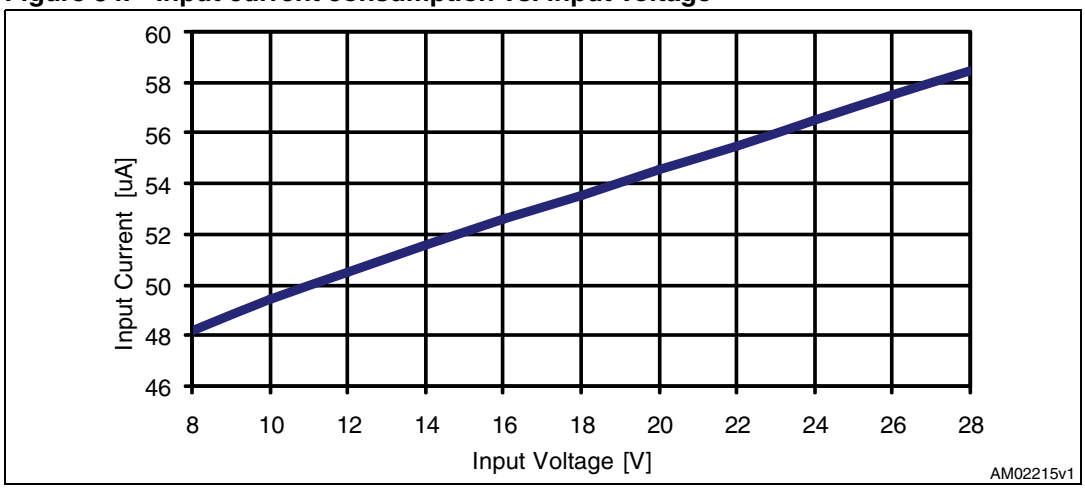


Figure 34. Input current consumption vs. input voltage



12 Revision history

Table 21. Document revision history

Date	Revision	Changes
19-Jun-2009	1	Initial release.

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